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PASSIVE GaAs FET SWITCH MODELS AND THEIR APPLICATION IN PHASE SHIFTERS

**L. Chainulu Upadhyayula, Raymond L. Camisa, Gordon Taylor,
S. N. Subbarao and S.G. Liu**

RCA Laboratories, Princeton, NJ 08543-0432

ABSTRACT

A new device model is proposed for the zero bias (V_{gs} = 0) and pinch off (V_{gs} = -V_p) states for GaAs MESFETs operated in a passive mode (I_{ds} = 0). The agreement between measurements and predicted S-parameter data is better than 90% which is 40-50% improvement over previously published models. The FET switch model will be discussed. The fabrication and performance of 12 GHz MMIC phase shifters designed using this new model will be described.

INTRODUCTION

Recently GaAs FETs have been increasingly used[1,2,3] as passive (I_{ds} = 0) control elements in phase shifters and SPDT switches operating at microwave frequencies. In this mode of operation when V_{gs} = 0 V the switch is in the low impedance or ON state and when $V_g < V_p$ it is in the high impedance or OFF state. Since dc drain current never flows, the power consumption is zero in both switch states. A small amount of drive power is required only during the transition between states to charge or discharge the input gate capacitance.

Ayasli[4], Fryklund and Walline[5] and Gutman et al[6] described FET switch models. These models are based on the dc or low frequency operation of the device. Diamond and Leviron[7] used the S-parameters of an FET to obtain accurate values for the equivalent circuit. Curtice and Camisa[8] extended this by including Fukui measurements to determine the series resistances. Fairly good agreement can be obtained between the measured and calculated S- parameters for 0 or small negative voltages on the gate. However, in the OFF state of the switch the difference between measured and calculated data is more than 20% for S11 and S22 and 30-40% for S21 and S12. In this presentation a new more accurate GaAs FET model for switch operation will be described for which better than 90-95% agreement has been achieved between the predicted and measured S-parameters. The device model, design, fabrication and performance of an X-band digital phase shifter will be reported.

Physical FET Model

A cross section of the FET under the operating conditions is shown in Fig. 1. when the gate bias is 0 V, there is very little depletion under the gate (Fig. 1a). Therefore, the FET can be modeled as a linear resistor (r) for currents less than the saturated channel current. The series resistances r_s and r_d due to the channel and ohmic contact regions are also shown here. The parasitic capacitances between drain-gate, source-gate and source-drain are not shown here for simplicity.

When a sufficient negative voltage is applied between the source and gate, the channel region under the gate is fully depleted of mobile charge carriers as shown in Fig. 1b. There exists a capacitance between source and drain due to this depletion region[9]. The depletion capacitance C is given by:

$$C = \frac{\varepsilon A}{h}$$

where h is depletion layer length and its value lies between the gate-length (lg) and the source-drain spacing (l_{sd}) depending on the FET fabrication, A is the area given by the thickness of the active layer times the gate width. This capacitance was not accounted for in earlier models which lead to erroneous results. This capacitance appears in parallel with the channel resistance which is of the order of several kilo-ohms as there is no conducting channel.

Also, in many switch applications the FET drain is not dc grounded and it is left floating. Therefore, the gate capacitance at the drain edge is different from that at the source edge. When the region under the gate is described by a distributed transmission line[7,8], the element values cannot be taken as identical. In our study we used up to 4 capacitor elements. However, we found that a 2-capacitor element circut adequately describes the FET switch under complete operating conditions.

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FET Switch Equivalent Circuit and Element Value Evaluation

The equivalent circuits for unbiased FETs with $V_g = 0$ and $V_g = V_p$ are shown in Fig. 2. Notice that $C_{g1} \neq C_{g2}$ in our case. Also, for $V_g = V_p$ an additional capacitance C appears across the high resistance ($\cong K\Omega$) channel. The drain-gate capacitance C_{dg}, the source-gate capacitance C_{gs} and the drain-source capacitance C_{ds} are fringing capacitances between electrodes and are estimated from expressions on interelectrode capacitance between parallel strips immersed in an infinite dielectric medium. The source and drain series resistances R_s and R_d respectively, are associated with the device structure and R_g is the gate resistance.

The proposed FET switch model has been verified using measured data on 0.75μm gate-length 0.6 mm gate width recessed gate type FETs fabricated in our laboratory. DC measurements described by Fukui were made to determine the resistances R_d, R_s and R_g. S-parameters were measured in the 8-18 GHz frequency range on an automatic network analyzer. Using S-parameter data the remaining circuit element values were optimized in the SUPER-COMPACT Computer program while minimizing the error function. The measured and computed S-parameter data are shown in Tables I and II for a typical G-26 device. The agreement is excellent. The element values obtained for several devices are given in Table III. Note that the capacitances C_{g1} and C_{g2} are substantially different for $V_g = 0$ as well as for $V_g = V_p$.

Digital Phase Shifters

Loaded line and switched line type 4-bit phase shifter circuits were designed for operation in the 11.5-12.5 GHz communication band with goals of 0-360° phase shift, less than 8 dB insertion loss and 1.5:1 input/output VSWR. The FET switch model described above was used in conjunction with the SUPER-COMPACT computer aided design program in optimizing the matching circuits for the phase shifter. Monolithic Microwave Integrated Circuits (MMICs) were fabricated on 5 cm ion-implanted GaAs substrates. The chip size of the individual phase shifter bit is $2.7 \times 1.7 mm^2$. The performance of the phase shifter bits were measured on the network analyzer. A photo micrograph of a loaded line phase shifter bit and its measured performance are shown in Figs 3 and 4. At 12 GHz a phase shift of 29° with 0.6 dB insertion loss and 1.7:1 VSWR were obtained. Similar performance was measured on the 45°, 90°, and 180° phase shifter bits. These results are in good agreemment with the design.

CONCLUSIONS

A new FET model was proposed for control element applications. S-parameter data was used to obtain element values in the equivalent circuits for $V_g = 0$ and V_p. A 4-bit digital phase shifter was designed, fabricated and tested. Good agreement was obtained between the design goals and measured results.

TABLE I. MEASURED AND COMPUTED S-PARAMETER DATA FOR $V_g = 0$ AND $V_{ds} = 0$ V

Freq.	S11		S21		S12		S22	
GHz	mag	ang	mag	ang	mag	ang	mag	ang
10.00	.941	176.6	.162	38.8	.166	38.2	.795	137.6
10.64	.913	172.4	.167	36.8	.165	37.0	.790	136.0
11.28	.911	170.4	.168	35.5	.170	35.3	.785	134.2
11.92	.910	166.3	.174	32.9	.172	32.8	.782	132.2
12.56	.894	164.2	.175	31.5	.177	31.5	.782	131.3
13.20	.906	160.2	.182	28.7	.181	28.5	.794	129 3
13.84	.892	157.8	.186	27.5	.187	27.4	.804	129.8

I(a) Measured Data

Freq.	S11		S21		S12		S22	
GHz	mag	ang	mag	ang	mag	ang	mag	ang
10.00000	.871	-178.2	.146	34.1	.146	34.1	.815	145.8
10.64000	.870	178.3	.150	33.3	.150	33.3	.817	143.7
11.28000	.870	175.0	.155	32.5	.155	32.5	.818	141 7
11.92000	.870	171.9	.159	31.6	.159	31.6	.820	139.7
12.56000	.870	168.9	.164	30.7	.164	30.7	.822	137.8
13.20000	.870	166.1	.168	29.8	.168	29.8	.823	135.8
13.84000	.870	163.4	.172	28.9	.172	28.9	.825	133.9

I(b) Computed data from the circuit model

TABLE II. MEASURED AND COMPUTED S-PARAMETER DATA FOR $V_g < V_p$ and $V_{ds} = 0$ V

Freq.	S11		S21		S12		S22	
GHz	mag	ang	mag	ang	mag	ang	mag	ang
10.00	.946	-131.9	.380	-20.5	.386	-19.9	880	-86 5
10.64	.922	-134.0	.388	-23.2	.387	-24.2	.909	-91.1
11.28	.915	-136.3	.380	-26.3	.381	-26.4	.881	-94.1
11.92	.912	-138.4	.390	-29.2	.389	-29.8	.913	-98.0
12.56	.904	-140.7	.384	-33.0	.383	-32.9	.878	-102.9
13.20	.925	-142.2	.394	-35.3	.394	-35.3	.893	-105.8
13.84	.928	-144.1	.392	-38.7	.394	-39.0	.871	-111.3

II(a) Measured Data

Freq.	S11		S21		S12		S22	
GHz	mag	ang	mag	ang	mag	ang	mag	ang
10.00000	.868	-125.5	.408	-14.5	.408	-14.5	.876	-83.1
10.64000	.868	-131.0	.403	-19.5	.403	-19 5	.877	-88.4
11.28000	.869	-136.0	.397	-24.5	.397	-24.5	.880	-93.7
11.92000	.871	-140.7	.388	-29.4	.388	-294.	.883	-99.0
12.56000	.874	-145.2	.377	-34.2	.377	-34.2	.877	-104.4
13.20000	878	-149.6	.365	-38.9	.365	-38.9	.892	-109.8
13.84000	.883	-153.9	.351	-43.6	.351	-43.6	.897	-115 3

II(b) Computed data from the circuit model

TABLE III. FET PARAMETERS FOR 0.75μm GATE LENGTH & 600 μm GATE WIDTH DEVICES

DEVICE	L_g(nH)	R_g(Ω)	C_{g1}(pF)	C_{g2}(pF)	R(Ω)	R_d(Ω)	L_d(nH)	R_s(Ω)	L_s(nH)
G26X2 VO	140	1.15	.945	.202	3.07	2.0	.196	.45	.057
G26X4 VO	.145	0.63	.745	.341	2.58	0.88	.205	.95	.055
G26X2 VP	.140	1.15	.087	.267	3.31K	2.0	.196	45	.057
G26X4 VP	.145	0.63	.084	.251	3.67K	.88	.205	.95	.055
A6X2 VP	.20	1 08	.038	.148	8.43K	2.91	.240	.558	.026
A6X3 VP	.20	1.238	056	131	9 15K	2.80	.240	.807	.026

C = 0.03 pF; C_{gd} = 0.054 pF; C_{gs} = 0.054 pF; C_{ds} = 0.084 pF

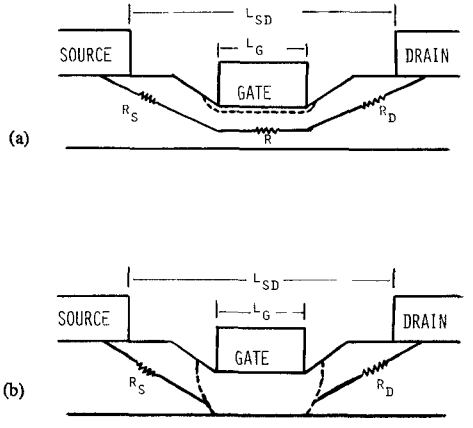

Figure 1. Schematic Cross Section of a GaAs FET Control Element. (a) $V_g = 0$ and (b) $V_g < V_p$.

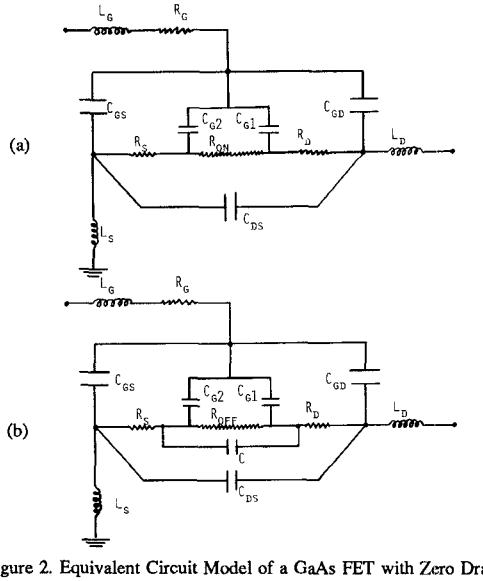

Figure 2. Equivalent Circuit Model of a GaAs FET with Zero Drain Bias. (a) for $V_g \approx 0$ and (b) for $V_g < V_p$.

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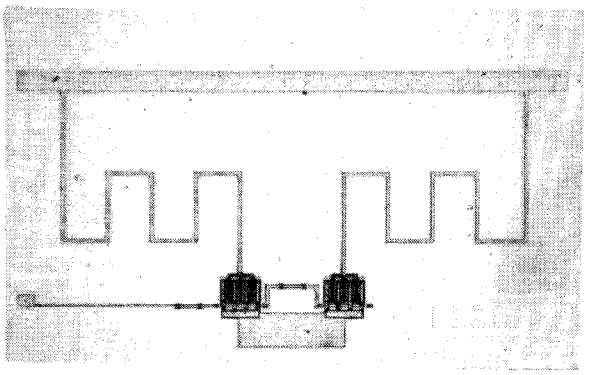

Figure 3. Photomicrograph of a fabricated loaded line phase shifter bit. Chip size is 2.7 x 1.7mm^2.

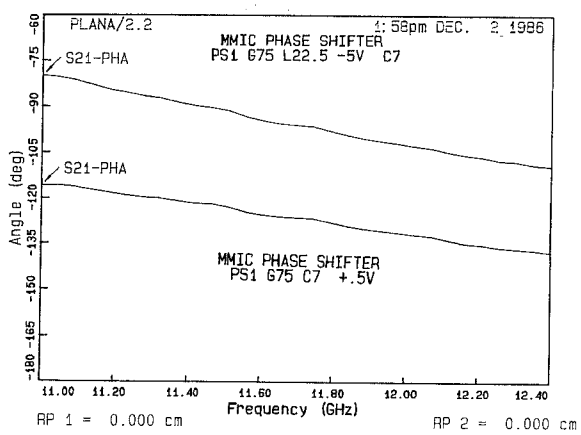

Figure 4. Measured phase response of a 22.5° loaded line phase shifter bit for the two states of the FET switches.